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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/768,065	02/02/2004	Shigetaka Aoki	60188-740	6161

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EXAMINER	
DOLAN, JENNIFER M	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 03/30/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/768,065	AOKI ET AL.	
	Examiner	Art Unit	
	Jennifer M. Dolan	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 December 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6 and 17-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 17-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 10/326,059.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-4 and 6 are rejected under 35 U.S.C. 102(b) as anticipated by Japanese Patent Publication 2001-319935 to Shiono et al. (cited by applicant).

Regarding claim 1, Shiono discloses a semiconductor device (figure 1) comprising: a single crystalline underlying layer (3, 4 paragraph 0021) formed in part of a substrate (1,3); an insulating layer (6; paragraph 0022) formed in another part of the substrate (figures 1, 2c); a semiconductor layer (10) epitaxially grown above the underlying layer (paragraph 0024) having a composition intersecting the claimed range (see paragraph 0023); a buffer layer (9) epitaxially grown (see paragraph 0024) between the underlying layer and semiconductor layer (figure 1) and having a composition intersecting the claimed range (see paragraph 0023), where the buffer layer has a greater quantity of Si than the semiconductor layer (see paragraph 0023; buffer layer has as Ge composition of 0-0.05, whereas the semiconductor layer has a Ge composition of 0.05-1); and a polycrystalline semiconductor layer formed on the insulating layer and having the same composition as the buffer layer (portion of 9 on layer 6) and semiconductor layer (portion of 10 on layer 6; also see paragraph 0026 – portion of 9 and 10 in window = single crystal

semiconductor, and portion on insulating layer 6 = polycrystalline semiconductor). It is inherently the case that polycrystalline silicon grown directly on an insulating layer will experience a time lag in the start of growth, thus causing the polycrystalline layer to have a smaller thickness than the corresponding single crystal silicon layer, and a polycrystalline layer grown on another polycrystalline layer will experience the same growth rate as the corresponding single crystal layer (see Applicant's specification, page 6, lines 1-15, page 7, lines 7-18; page 19, lines 1-10; figure 18). Hence, since Shiono discloses forming the first semiconductor film and buffer layer in a single step, where the first film is formed directly on the insulating layer, and the second semiconductor film and the semiconductor layer in a single step, overlying the first film and the buffer layer, respectively, it must be inherently the case that the thickness of the first semiconductor film is less than that of the buffer layer, whereas the second semiconductor film and the semiconductor layer must inherently have about the same thickness.

Regarding claim 2, Shiono discloses that the single crystalline underlying layer is Si (3; paragraph 0021).

Regarding claim 3, Shiono discloses that the semiconductor layer and polycrystalline layer are SiGe (10; paragraphs 0023-0026), the buffer layer is a Si layer (layer 9 includes x=0 condition, which corresponds to a pure Si layer; see paragraphs 0023-0026; 0033).

Regarding claim 4, Shiono discloses that the underlying layer is a collector layer (layer 3, including regions 4 and 5, acts as a collector – see description of notations section; the semiconductor layer has at least part serving as a base layer (11) and wherein the polycrystalline semiconductor layer serves as at least part of a base lead electrode (see figure 1; polycrystalline

portion (left-most portions of layer 10) connects base region and base electrode (20)), the device functioning as a heterojunction bipolar transistor (see paragraphs 0019, 0021, etc).

Regarding claim 6, Shiono discloses a buffer layer thickness intersecting the claimed range (paragraph 0024).

3. Claims 1-4 and 6 are rejected under 35 U.S.C. 102(a) as being anticipated by Japanese Patent Publication 2002-026027 to Yokoyama et al (cited by applicant).

Regarding claims 1-3, Yokoyama discloses a semiconductor device (figure 6) comprising: a single crystalline underlying silicon layer (112, 113; paragraph 0011) formed in part of a substrate (111, 112; see figure 6); an insulating layer (110) formed in another part of the substrate (paragraph 0011); a semiconductor layer (132) epitaxially grown (paragraph 0014) above the underlying layer and being formed of SiGe (paragraph 0014); a buffer layer (121) epitaxially grown between the underlying layer and semiconductor layer, having a Si composition (paragraph 0014); and a polycrystalline semiconductor layer (133, 122) formed on the insulating layer (figure 6) and having the same composition as the buffer layer (portion 122; see paragraph 0014) and a semiconductor (133) having the same composition as the semiconductor layer (paragraph 0014). Since Yokoyama discloses forming the first semiconductor film and buffer layer in a single step, where the first film is formed directly on the insulating layer, and the second semiconductor film and the semiconductor layer in a single step, overlying the first film and the buffer layer, respectively, it must be inherently the case that the thickness of the first semiconductor film is less than that of the buffer layer, whereas the second

semiconductor film and the semiconductor layer must inherently have about the same thickness, for the same inherency reasons as listed in the rejection using Shiono et al.

Regarding claim 4, Yokoyama discloses that the underlying layer is a collector layer (paragraph 0012; layers 113 and 131 form collector); the semiconductor layer has at least part serving as a base layer (paragraph 0012 – layers 121 and 132 form the base region); and wherein the polycrystalline layer serves as part of a base lead electrode (portion 133) connects base to the base electrode (see paragraph 0013), the device functioning as a HBT (see paragraph 0019; device is a BJT using Si/SiGe heterojunctions, and thus is a HBT.

Regarding claim 6, Yokoyama discloses that the buffer layer thickness is 10 nm (paragraph 0014).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shiono et al. in view of U.S. Patent No. 6,551,891 to Chantre et al.

Shiono discloses that the methods for forming the polycrystalline SiGe layer on the insulator layer can be applied to forming a gate electrode on a gate oxide for a MIS transistor (paragraph 0036). Shiono fails to specifically suggest forming a BiCMOS device where the same polycrystalline semiconductor layer is used as a base layer can be used as a gate electrode.

Chantre teaches a BiCMOS device wherein the same silicon oxide film is used as the HBT isolation film and the MIS gate oxide, and wherein polycrystalline layers are deposited upon the silicon oxide film to form the gate electrode and the base (see column 4, lines 30-37).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Shiono and Chantre, such that a BiCMOS layer is formed, using the polycrystalline semiconductor layer as a gate electrode. The rationale is as follows: A person having ordinary skill in the art would have been motivated to use the polycrystalline semiconductor layer as a gate electrode of a MIS in a BiCMOS, since Shiono specifically teaches that the same techniques for forming a base-lead of a HBT can be applied to formation of a gate electrode of a MIS transistor (Shiono, paragraph 0036), and Chantre specifically teaches that the same silicon oxide film is used as the HBT isolation film and the MIS gate oxide, where the base-lead polysilicon film and the gate electrode polysilicon film are formed directly thereon (Chantre, column 4, lines 30-37). Hence, using the polycrystalline semiconductor layer as the gate electrode would enable formation of the base region, the base-lead, and the gate electrode in the same process step, thus decreasing the complexity of fabrication of the device.

6. Claims 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yokoyama et al. in view of U.S. Patent No. 6,346,453 to Kovacic et al.

Yokoyama fails to disclose the polycrystalline silicon film covering the polycrystalline semiconductor layer.

Kovacic discloses a HBT structure similar to that of Yokoyama, including a polycrystalline silicon film (120, 220; also listed as "p+ Si" in figure 24 or "p+ Si poly" in

figures 22 and 23, or "p+" in figures 12-13) covering the polycrystalline semiconductor layer (portion of Si/SiGe layer 112, 114, 212, 214 disposed over the field oxide or STI) and connected to the semiconductor layer (portion of 112, 114, 212, 214 not disposed over the field oxide or STI in figures 12-13 and 19-24) at an edge of the polycrystalline semiconductor layer (see figures 12-13 and 19-24), and including a sidewall oxide layer at each sidewall of the polycrystalline silicon film (122, 222; see figures 13; 23, 24; column 7, line 3 – column 8, line 13).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the HBT structure of Yokoyama, such that it includes the polycrystalline silicon film with sidewalls taught by Kovacic. The rationale is as follows: A person having ordinary skill in the art would have been motivated to provide a polycrystalline silicon film overlying the polycrystalline semiconductor layer, because Kovacic shows that such a film can be used as a base electrode lead, thus enabling the base layer to remain very thin, which improves the response time of the transistor, while minimizing the contact resistance of the base electrode and the resistance of the polysilicon connector between the base electrode and the single crystal base layer (see Kovacic, column 1, lines 14-50). A person skilled in the art would further use oxide layers on the sidewalls of the polycrystalline silicon film, because doing so isolates the base electrode from the emitter electrode, as is appreciated by a person having ordinary skill in the art.

Response to Arguments

7. Applicant's arguments filed 12/28/05 have been fully considered but they are not persuasive.

The Applicant states that claim 1, as amended, requires that "the first semiconductor film has a thickness smaller than the buffer layer and the second semiconductor film has substantially the same thickness as the semiconductor layer," and cites page 18, line 20 – page 19, line 10 and page 20, line 25-page 21, line 4 as support for this new limitation. The Applicant argues that Shiono, Yokoyama, and Chantre do not disclose layer dimensions meeting this limitation.

Regarding Shiono and Yokoyama, the Examiner disagrees with this assessment. The only disclosure of the relative thicknesses of the buffer layer and the polycrystalline semiconductor film in the Applicant's specification suggests that in any circumstances wherein a semiconductor layer is epitaxially grown upon a substrate including single crystalline regions and insulation film regions, the film grown upon the insulation regions will experience a time lag before the start of layer growth (during which growth nuclei are formed on the insulation film until a critical density is formed - see specification, page 6, lines 1-16, page 7, lines 7-18; page 19, lines 1-10; figure 18). Subsequently grown layers will grow at the same rate on the single crystalline and polycrystalline surfaces. Insofar as the specification is understood by the Examiner, the time lag in growth is considered to be a generally undesirable effect that the Applicant appears to be minimizing, so as to allow for uniform growth of the subsequent polycrystalline SiGe layer upon the Si layer, while enabling formation of a relatively thin buffer layer. Since Shiono and Yokoyama disclose forming the buffer layer and polycrystalline Si layer directly on the insulating layer through methods similar to that of the Applicant and without

taking any particular steps to provide a seed layer or a starting growth nuclei density, it is expected that the polycrystalline Si layer in Shiono and Yokoyama would experience the same time lag in growth as that disclosed by the Applicant, and that subsequently grown layers would not experience a time lag. Thus, Yokoyama and Shiono must inherently have polycrystalline Si layers with a smaller thickness than the single crystal buffer layer, and polycrystalline SiGe layers with the same thickness as the single crystal SiGe layer, and hence, they anticipate the claimed subject matter of claims 1-4 and 6.

In contrast, Chantre specifically does teach formation of a seed layer to enable growth of the polycrystalline layer on the isolation film layer, and hence, it is expected that the buffer layer and corresponding polycrystalline silicon layer will grow at the same rate and have the same thickness. Thus, the Examiner has withdrawn the anticipation rejections using Chantre.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Dolan whose telephone number is (571) 272-1690. The examiner can normally be reached on Monday-Friday 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W. Whitehead, Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jennifer M. Dolan
Examiner
Art Unit 2813

jmd